**AMENDMENTS TO THE DRAWINGS**

Fig. 5 is amended to include a reference numeral 7 for the lead wire of the capacitor 1. Further, the specification at page 24 has been amended to include a description of the lead wire 7. Particularly, this is representative of the Ta lead wire of Example 1 as described bridging pages 24-25 of the specification. No new matter has been added.

Fig. 6 illustrates the energization of the embodiment of Example 1 for forming a semiconductor layer on sintered body 8, the sintered body 8 including lead wire 7 embedded in electric conductor 2 having formed on the surface thereof dielectric layer 3 and further including fine protrusions (not shown) formed on the dielectric layer 3. The sintered body 8 is dipped into electrolytic solution (semiconductor layer - forming solution) 11, and a positive terminal of direct current source 10 is electrically connected to the lead wire 7 and a negative terminal of the direct current source is electrically connected to a negative electrode plate 9 disposed in the electrolytic solution, to thereby pass a direct current between the lead wire 7 and the negative electrode plate 9. The sintered body is described at page 24, line 26 - page 27, line 10. Energization for forming the semiconductor layer is described at page 27, lines 11-23 of the specification. No new matter has been added.

Enclosure: 1 Annotated Sheet (Fig. 5)
1 Replacement Sheet (Fig. 5)
1 New Sheet (Fig. 6)

## REMARKS

**Interview Statement:**

Applicants appreciate the Examiner's courtesy in granting the telephone interview of October 11, 2011 with the undersigned. A proposed amendment to claims 21 and 22 (the same amendment as presented herein) as well as new claims 28 and 29 were submitted as a basis for discussion. Particularly, Fig. 3 and paragraph [0052] of Yoshida et al were discussed, and the undersigned pointed out distinctions between the invention and the prior art (noting that in the invention a positive potential is applied to the electric conductor having thereon the dielectric layer, whereas in Yoshida et al, the film formation substrate 10 is positioned between the electrodes 7 and 8).

The Examiner agreed that the proposed amendments to claims 20 and 21 distinguish over Yoshida et al. However, when filing a response to the outstanding Office Action, the Examiner requested submission of a new drawing (Fig. 6) for addition to the specification which illustrates the features of the invention as specified in claims 20 and 21. Further, the Examiner requested submission of amended Fig. 5 which labels the lead wire, together with conforming amendments to the specification.

**Response to Office Action:**

In response to the Examiner's request, Fig. 5 has been amended to label the lead wire, and conforming amendments have been made to the specification. Further, Applicants submit herewith Fig. 6 for addition to the specification which illustrates the energization of the embodiment of Example 1 for forming a semiconductor layer on sintered body 8. Fig. 6 illustrates the energization of the embodiment of Example 1 for forming a semiconductor layer

on sintered body 8, the sintered body 8 including lead wire 7 embedded in electric conductor 2 having formed on the surface thereof dielectric layer 3 and further including fine protrusions (not shown) formed on the dielectric layer 3. The sintered body 8 is dipped into electrolytic solution (semiconductor layer - forming solution) 11, and a positive terminal of direct current source 10 is electrically connected to the lead wire 7 and a negative terminal of the direct current source is electrically connected to a negative electrode plate 9 disposed in the electrolytic solution, to thereby pass a direct current between the lead wire 7 and the negative electrode plate 9. The sintered body is described at page 24, line 26 - page 27, line 10. Energization for forming the semiconductor layer is described at page 27, lines 11-23 of the specification. No new matter has been added.

The specification has also been amended to include a description of the drawing (Fig. 6). This drawing is submitted pursuant to 37 C.F.R. § 1.83. No new matter has been added.

Claims 5-21 and 23-27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Publication No. US 2003/0133256 A1 to Yoshida et al. In particular, the Examiner relies on Yoshida et al as disclosing the limitation of passing an electric current through the electric conductor having formed on the surface thereof the dielectric layer using the electric conductor as an anode, citing paragraph [0052]. The Examiner commented as follows:

> (Examiner notes that the energization process is shown in fig. 3-7 where 10 represents the anode conductor with a dielectric layer thereon immersed in polymerization solution with a power supply (12) present, there is current flow through solution and the anode conductor 10);

In the Response to Arguments bridging pages 10-11, the Examiner further commented that Applicants have not claimed the structural difference between the invention and Yoshida, where Yoshida et al is said to teach that the electric conductor is used as an anode.

The above rejection should be withdrawn because the film formation substrate 10 in Yoshida et al is arranged so that it is disposed between the electrodes 7 and 8 (where the film formation substrate 10 is separate from the anode 7, which is connected to the positive electrode terminal (+) of the power source), such that no electric current is passed through the film formation substrate 10.

Further, the term "anode" as used in the present claims designates the positive polarity contact, differing from the polymerization anode (positive electrode) 7 of Yoshida et al.

As to the first issue, the Examiner takes the position that because there is current flow through the solution, there is also current flow through the anode conductor 10. Applicants disagree. As shown in Fig. 3 of Yoshida et al, the film formation substrate 10 is not grounded and is not connected to any circuit either. Therefore, even though there is current flow through the solution, no electric current passes through the film formation substrate 10 as understood by those skilled in this field of art.

As to the above second issue, Applicants amend claims 20 and 21 so as to distinguish the electric conductor having formed on the surface thereof a dielectric layer and to which a positive potential is applied from the polymerization anode (positive electrode) 7 of Yoshida et al. Support is found, for example, at page 27, lines 11-23 of the specification. As recited in claims 28 and 29, the applying step comprises connecting the electric conductor having formed on a surface thereof a dielectric layer to a positive terminal of the power supply and connecting the negative electrode to a negative terminal of the power supply.

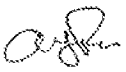
It is respectfully submitted that the claims as amended patentably distinguish over Yoshida et al, and withdrawal of the foregoing rejection under 35 U.S.C. § 103(a) is respectfully requested.

Withdrawal of all rejections and allowance of claims 5-21 and 23-29 is earnestly solicited.

In the event that the Examiner believes that it may be helpful to advance the prosecution of this application, the Examiner is invited to contact the undersigned at the local Washington, D.C. telephone number indicated below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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